

Why *Analog* Silicon may be the best solution For LCOS Digital TV

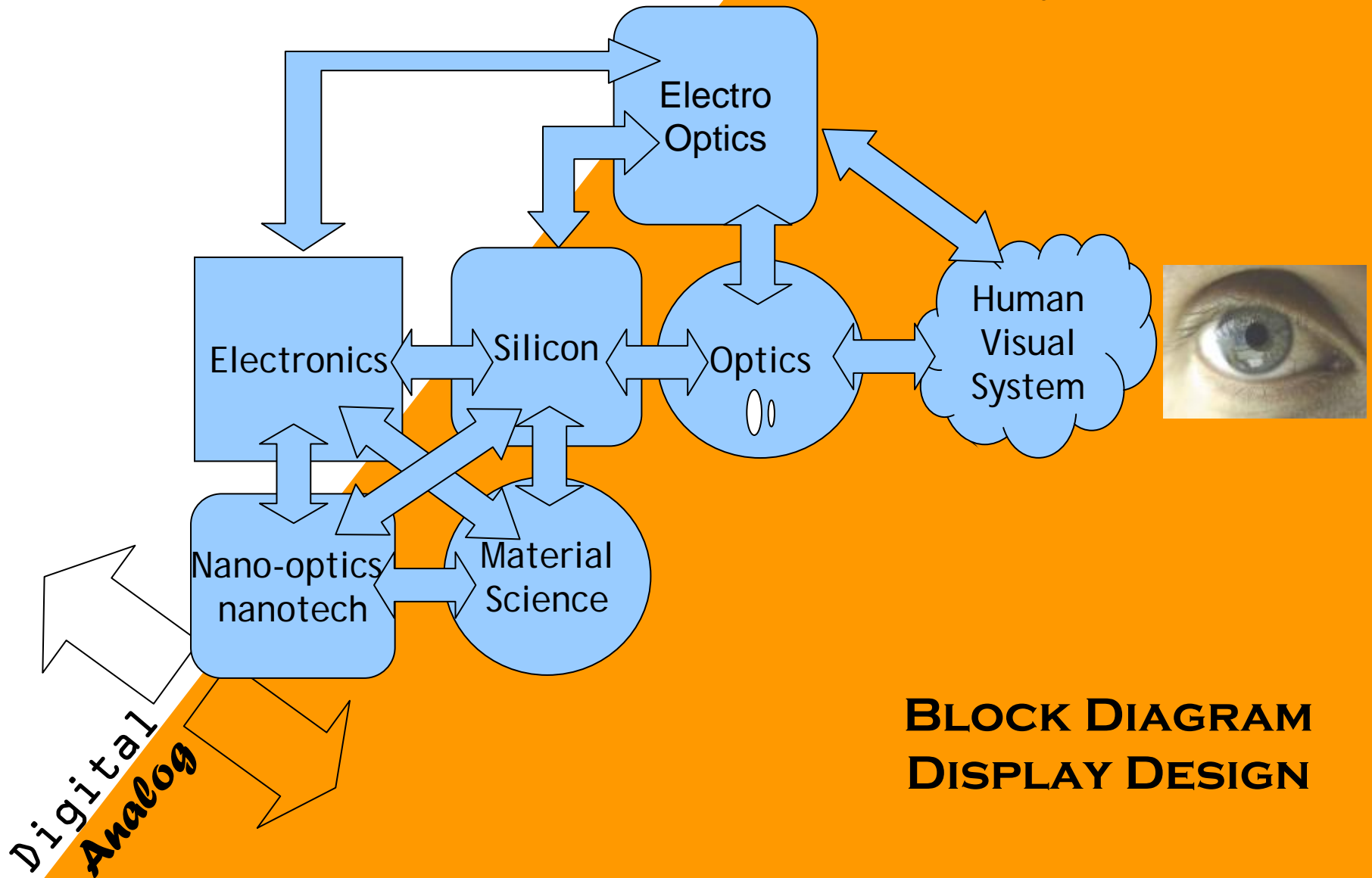


Dr. Mary Lou Jepsen
2005 Annual SID Symposium
Boston, Mass



Now with:
Hundred Dollar Laptop Corp.,
MIT Media Lab and JOE, Inc.
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Digital *Analog*



**BLOCK DIAGRAM
DISPLAY DESIGN**

How do we get displays to follow Moore's Law?

Why does it take so long from first demo to mass production in display?

Can't we use the IC industry as a role model?



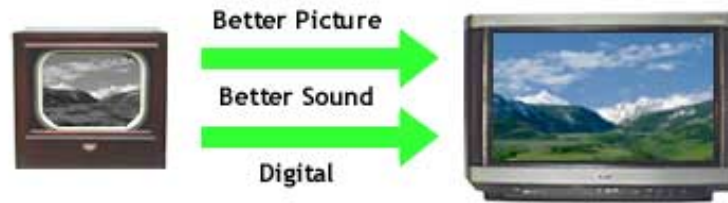
Isn't Digital Better?

Digital
Analog

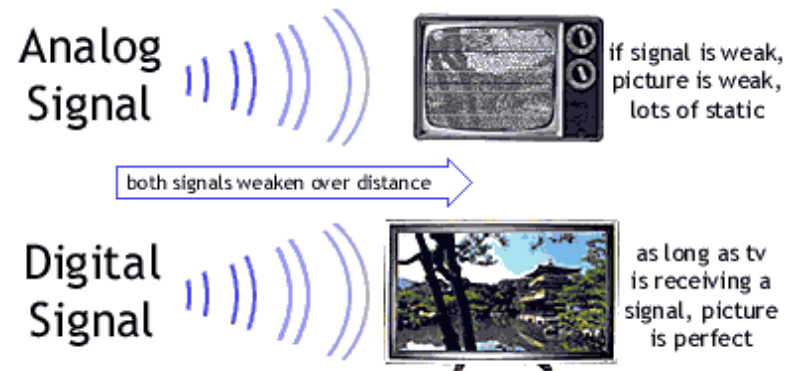
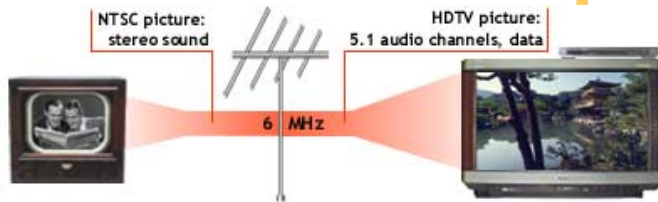
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Why is Digital TV is Considered Better



Noise-Free



But this is the signal... Digital TV describes the signal into the TV

Digital
Analog

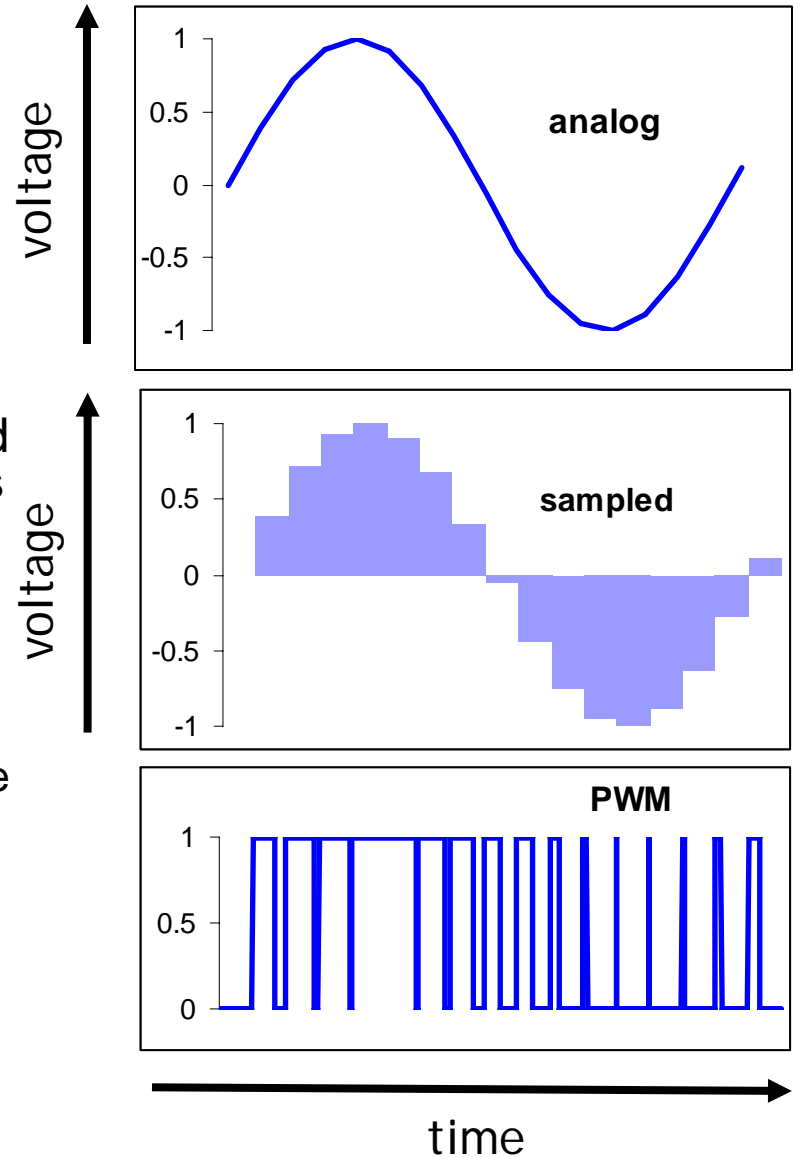
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What is Digital? Analog?

All 3 signals are sinusoid but...

- Silicon processes can be optimized for
 - rail-to-rail (aka Digital)
 - time domain only, or (Digital)
 - voltage and time domain (Analog)
- Silicon Process Selection should be based on price/performance and include analysis on:
 - transistor density required
 - Silicon area required
 - thermal design management req by higher frequencies
 - liquid crystal response time – and response shape
 - Ultimately: lumens/dollar



Digitals
Analog

voltage

Silicon Process Selection

Yields

$$Y = e^{-\sqrt{\frac{A}{A_0}}}$$

Defect density * Die Area

Sensitivity to defects (process feature size, transistor design density, wafer diameter)

$$DieYield = \exp\left(-\frac{N_{tran} d_{density} D}{\lambda^{(p-2)}}\right)$$

Where:

N_{tran} = NumberOfTransistorsInDie

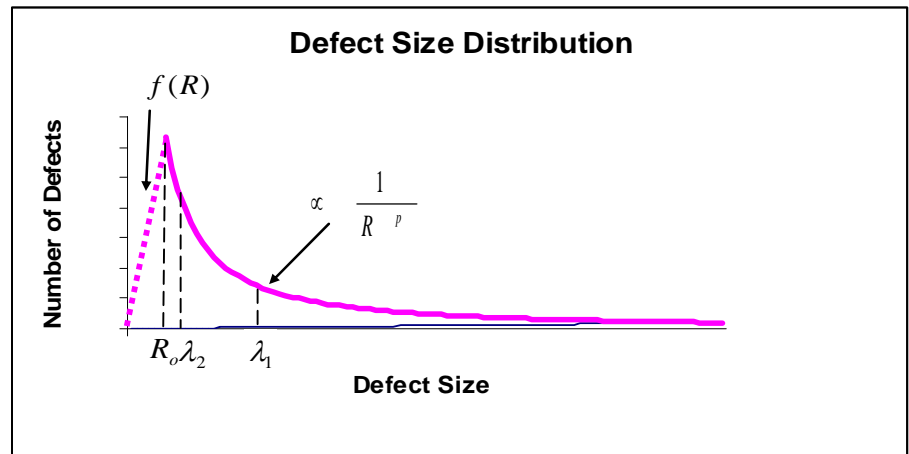
$d_{density}$ = InverseOfNumberOf

MinimumFeatureSizeSquaresInAverageTransistor

D = DefectDensity

p = DefectCharacterizationParameter(4-5)

λ = MinimumFeatureSize



KEY POINT: Trailing edge are better yielding

Digitals
Analog

Silicon Process Selection

2004 ASPs

Wafer size	Line-width (μm)	Mask layers				
		18	20	22	24	26
200mm	0.5	\$615	\$675	-	-	-
	0.35	\$700	\$760	\$830	-	-
	0.25	\$890	\$980	\$1,070	\$1,155	-
	0.18	-	\$1,320	\$1,440	\$1,565	-
	0.13	-	-	\$1,815	\$1,970	\$2,130

src: ICKnowledge.com

KEY POINT: Trailing edge (larger line-width processes) are also less expensive

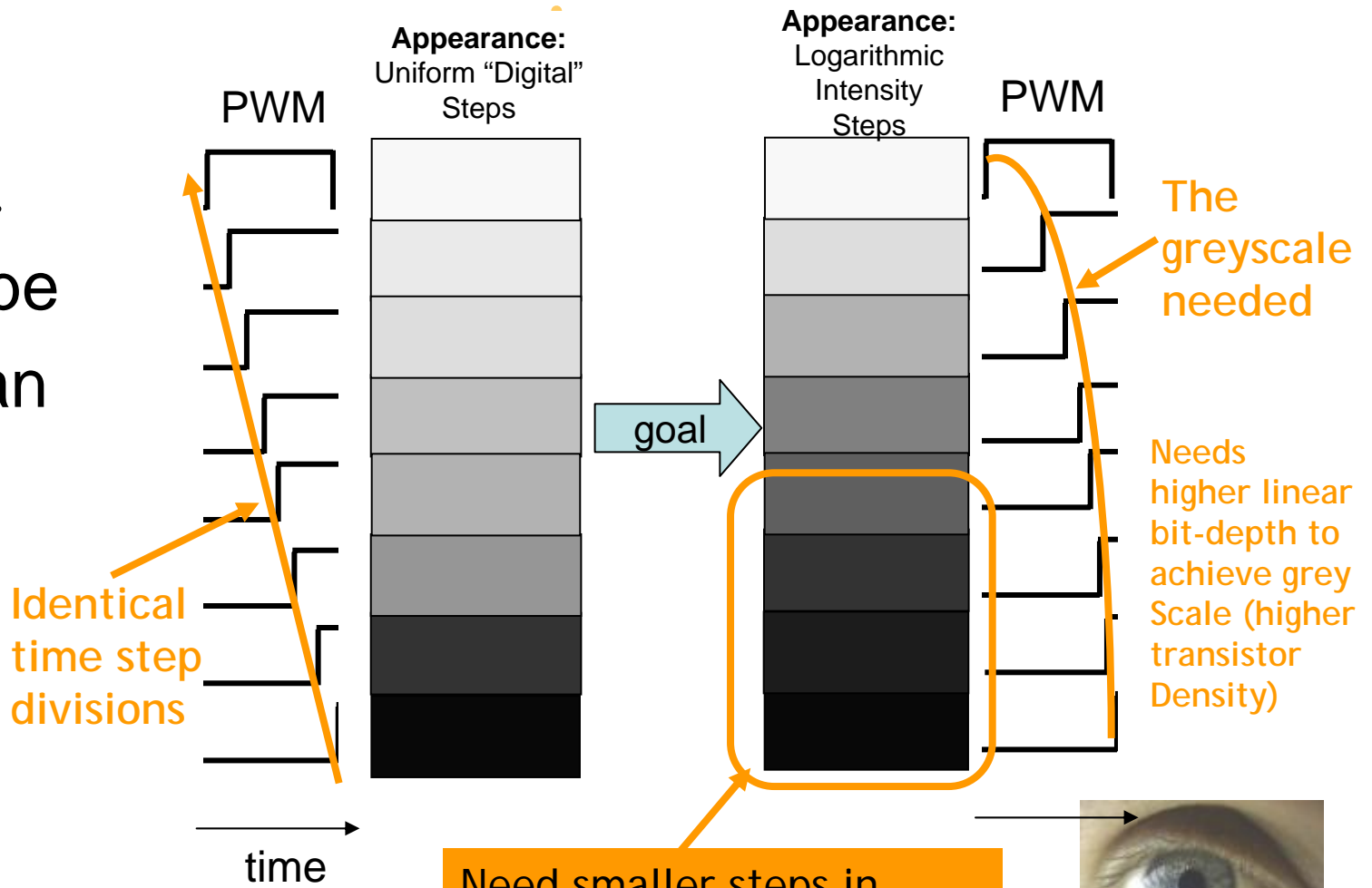
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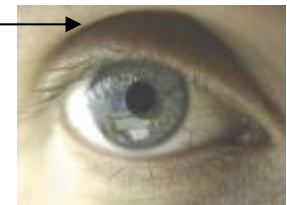
Digital Greyscale Encoding

Why
digital
may not be
better than
analog:



Digital
Analog

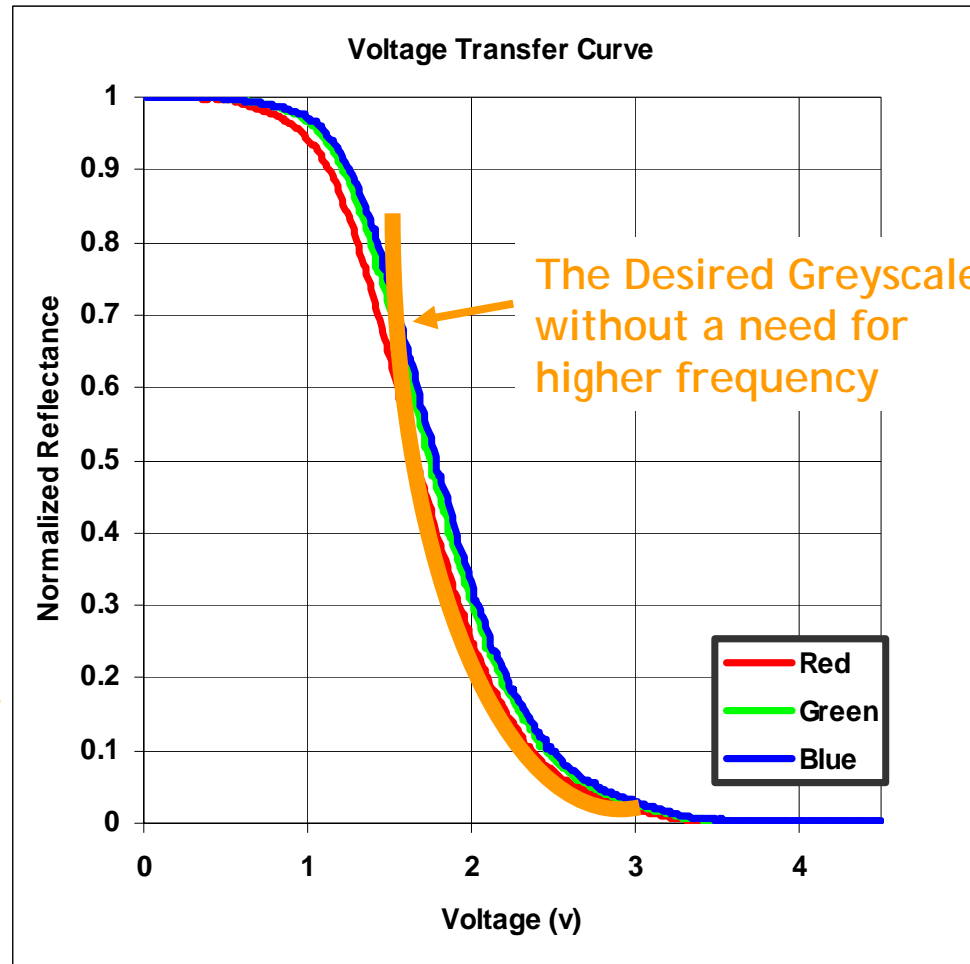
Need smaller steps in the blacks to get greyscale



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LC material response is *Analog*

and it matches the human visual system greyscale nearly perfectly



Temperature sensitivity (10C)

Digital
Analog

Main Goal: Best Lumens/Dollar at high image quality (not digital or analog)



Using Analog Silicon – So far

- + Lower design complexity (transistor density)
- + Lower bit depth (for same visual experience)
- + Lower clock speed (less power, thermal packaging)
- + Lower cost silicon wafers with trailing edge
- + Higher Yield

Analog Silicon has substantial cost advantage over digital processes
→ In a world where silicon shrink isn't possible (etendue)

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Analog

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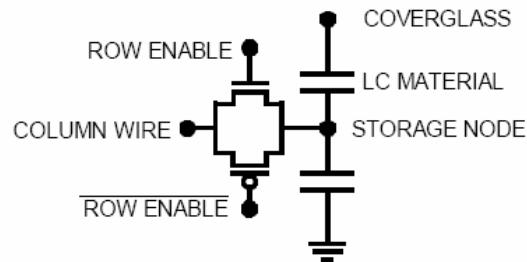


Transistor Density

Survey of LCOS design published literature showed

- *Average* analog design 12T/pixel.
- *Best* in class digital design was 24T/pixel
many designs were far more dense

Schematic



ANALOG

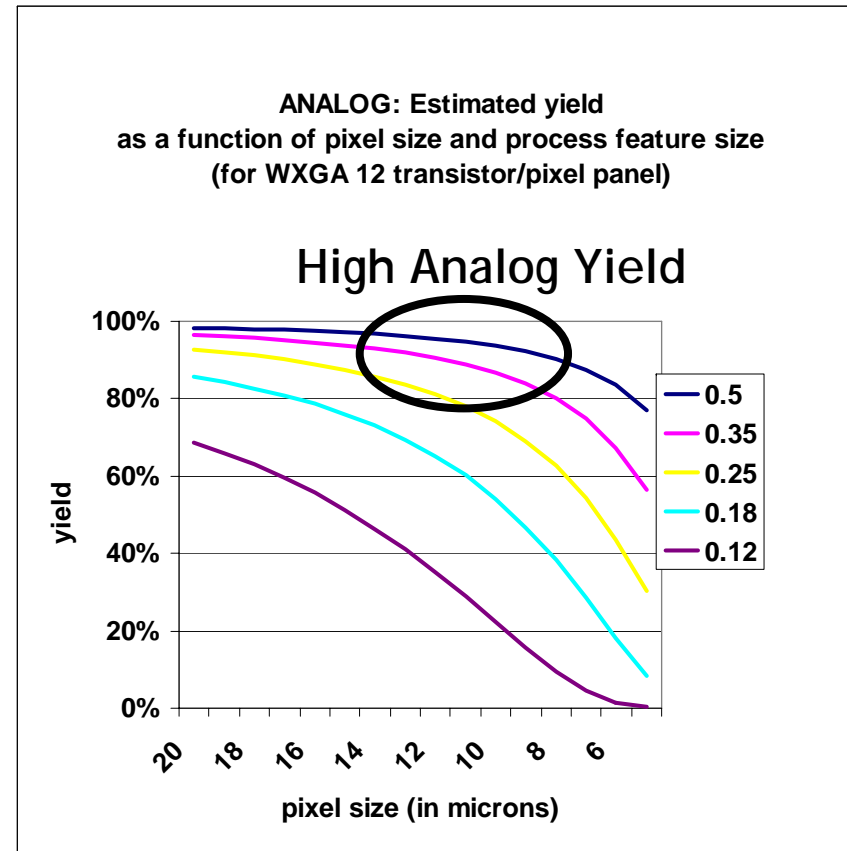
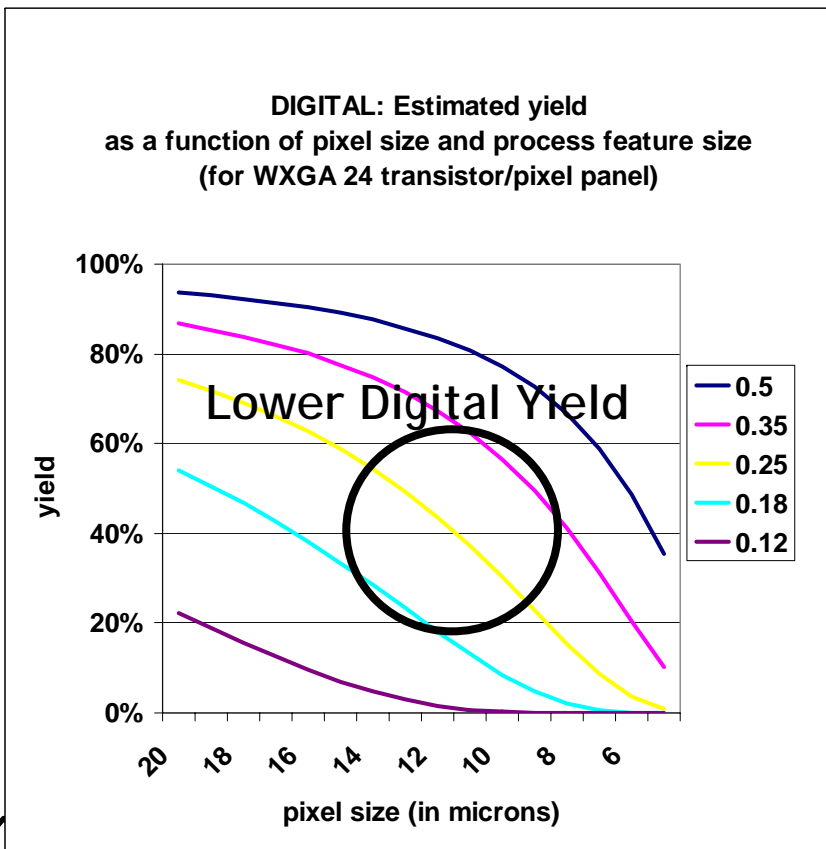
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Silicon Backplane Yield

Using the data presented on the past slides, and the basic yield Formula presented we arrive at yield estimates



Relative Estimated Costs

0.35 micron process										
12 transistors/pixel Analog	1280x720					1920x1080				
pixel array diagonal (in inches)	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
Silicon yield Estimate	95%	93%	91%	88%	83%	76%	70%	63%	53%	41%
die per wafer (w/ 2mm border)	76	92	114	144	187	76	92	114	144	187
yielded die per wafer (dpw)	72	86	104	127	156	58	64	72	77	76
LC Assembly yield (gross estimate)	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$
Wafer Cost (gross estimate)	wafer cost									
wafer level LCA cost	wafer level assembly cost									
die level cost (packaging, test cost per die)	$\beta * \text{number of die}$									
Relative Panel Cost	1.4	1.2	1.0	0.9	0.8	1.7	1.4	1.2	1.1	1.1

0.25 micron process					
24 transistors/pixel PWM	1280x720				
pixel array diagonal (in inches)	0.9	0.8	0.7	0.6	0.5
Silicon yield Estimate	63%	56%	47%	35%	22%
die per wafer (w/ 2mm border)	76	92	114	144	187
yielded die per wafer (dpw)	48	51	53	51	41
LC Assembly yield (gross estimate)	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$
Wafer Cost (gross estimate)	wafer cost				
wafer level LCA cost	wafer level assembly cost				
die level cost (packaging, test cost per die)	$(\beta + \text{thermal}) * \text{number of die}$				
Relative Panel Cost	2.7	2.4	2.2	2.2	2.3

The larger problem comes in digital designs of higher resolution - even 2Mpixel in this model presented a problem



Digit
Analog

Digital panel is about double the cost of the analog panel

Summary

- Analog Silicon LCOS panels with digital interfaces are about half the cost of Digital version with equivalent image quality
- Existence proofs of excellent analog image quality:
 - Movies Film
 - MicroDisplay LCOS
- Lumens/dollar is what matters, and for portable lumens/dollar/watt -> analog seems to provide a better solution

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