

P-39.1: Why Analog Silicon May Be Best For LCOS Digital TV

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... We used to have a scale from one to ten. This binary math is the modern way...

It's on or off, wrong or right. There is no gray, only black and white...

From 'Countin' On You' by Arlie Conner & Paula Conway

Abstract

Seemingly insignificant architectural silicon design choices can have a profound effect on both the performance and price of the liquid crystal on silicon (LCOS) device, and its optical system. The impact ranges from the obvious: silicon wafer yields and costs -- to the not-so-obvious: lumen throughput, engine cost, die packaging costs, panel uniformity and greyscale bit-depth.

Various LCOS panel architectures are compared. Through use of feature sizes, transistor densities, and die sizes - silicon backplane yields and thus die-level costs are estimated. Performance benefits such as greyscale reproduction, full-frame update, single-panel capabilities, pixel resolution and so forth are also compared. An estimate of total system price/performance is tabulated. These estimates indicate that analog backplanes (with digital interfaces, pixelated digital outputs, but continuous greyscale voltages optimized to liquid crystal voltage transfer curve) may currently offer best price with adequate performance for the rear projection television market.

1. Introduction

The reality of tremendous price pressure on consumer electronics components requires a focus on price/performance. The multidisciplinary effort required for LCOS components spans expertise in CMOS design and architecture, liquid crystals, chemistry, manufacturing process development, optics, the human visual system, and television signal encoding and transmission. While it is well known that optimization of each subsystem does not produce the optimal price/performance of the resultant system, this paper examines several LCOS architectures in detail inferring a gross approximation on relative cost and performance. The implication is that optimal design choices, even with respect to seemingly small issues at the silicon architecture level, should be made by a team with a broad expertise.

While mainstream silicon design assumes Moore's Law - enabled by ever improving silicon manufacturing processes - many LCOS silicon processes have changed little in the last 5 years. The rules that govern LCOS process improvement are different than those harnessed for other silicon products. For example:

1. Optimal die area is linked to the light source, and a large die allows substantially higher light throughput than a smaller die. This concept is known as *etendue*.
2. >3 volt backplane voltages are desired: the higher the backplane voltage the more available LC mode options; voltage *analog* control of the LC allows greyscale response that matches the human visual system and requires less bit depth than temporal-only-*digital*-modulation of the LC.
3. Low backplane power consumption reduces packaging costs (thermal dissipation requirements) and perhaps more importantly eases the challenge in maintaining display uniformity over time with a thermal load.

Thus, digital isn't necessarily better for microdisplay products.

2. Estimate of Silicon Yield and Cost

Some silicon foundries produce higher yields than others; such information is proprietary and is neglected in this analysis: instead a generic (and approximate) model of silicon yield is constructed. Defect distribution as a function of size can be modeled via a number of functions^{1,2}; the one most often used due to its simplicity is depicted below:

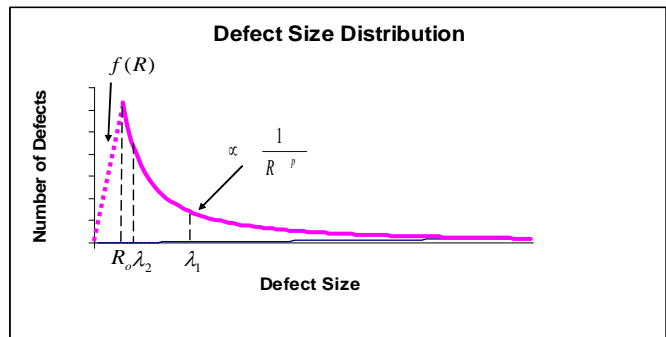


Figure 1: A typical defect size distribution as a function of number of defects. The peak number of defects are small in size and can be fatal to small feature sizes: creating either shorts or opens. The same small size defects are not fatal to larger feature and wire widths.

Using published defect densities, and estimated transistor density, gross silicon yield can be estimated using, for example, the Poisson Yield Model.^{3,4,5} The model assumes a uniform distribution of faults across the wafer:

$$DieYield = \exp\left(-\frac{N_{tran} d_{density} D}{\lambda^{(p-2)}}\right) \quad [1]$$

Where:

N_{tran} = NumberOfTransistorsInDie

$d_{density}$ = InverseMinFeatureSizeSquaresInAvgTransistor

D = DefectDensity

p = DefectCharacterizationParameter(4 – 5)

λ = MinimumFeatureSize

Using the above equations and varying a) the number of transistors per pixel and b) the pixel size for a 1280x720 device the following die yield is estimated for a 0.25 micron minimum feature size.

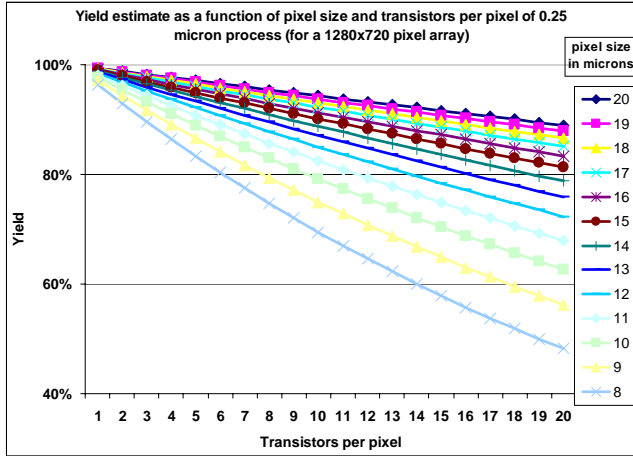


Figure 2: An estimate of silicon yield as a function of the number of transistors per pixel and the pixel size for a WXGA array. Note that the predicted silicon yield decreases as the silicon area decreases (here driven by pixel size), however, the number of die per wafer increase.

Similarly, the number of transistors per pixel is maintained as constant and the minimum feature size is varied. The yield thus decreases with a move to smaller feature sizes. Of course, more die per wafer can make up for this, but smaller die suffer from light-loss due to etendue. The net impact of lumens/dollar must be evaluated.

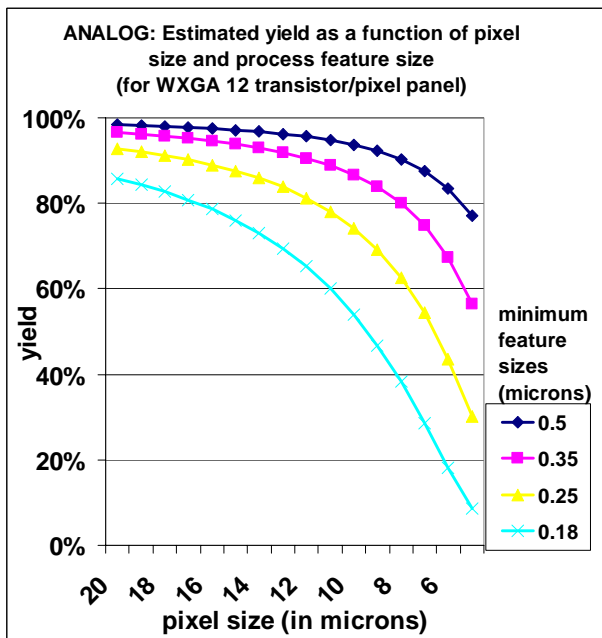


Figure 3: Example yield for a 12 transistor per pixel architecture. Assumes typical published analog LCOS architectures of ~12 transistor per pixel. Note: in an analog silicon process, the transistors aren't optimized for rail-to-rail, binary operation, but instead can modulate voltage. Analog silicon can still have a fully digital interface, and digitized, digital-pixels, but may use voltage modulation to better match to the material characteristics of the liquid crystal layer.

Digital, pulse width modulation (PWM), architectures need more transistors per pixel than an analog based DRAM style architecture. For an SRAM (the so-called digital silicon cells) rail-to-rail operation is used. A minimum of 4 transistors, and typically 6 transistors, are used per SRAM cell. Displaytech has published a 24-transistor-per-pixel PWM design as the minimum achievable transistor density for PWM.⁶ Using this figure we again plot our silicon yield estimates

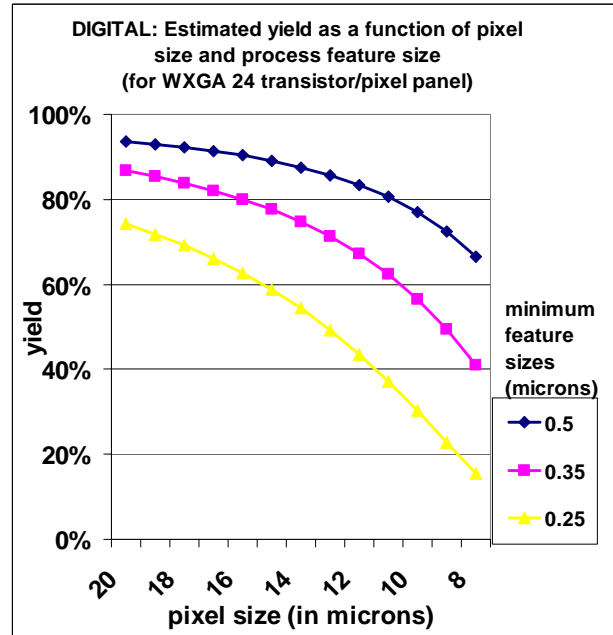


Figure 4: A higher transistor density is depicted and yield is estimated; this is the minimum polished density needed for pulse width modulation of the liquid crystal layer (as opposed to voltage modulation as is possible with DRAM cells). The yield is negatively impacted with higher transistor density.

Use of memory in the backplane can have a positive impact on lumen throughput in a single-chip field sequential color projection system, but there appears to be no increased brightness from backplane memory for triple panel projection systems. Backplane designs that include memory can more than double the number of transistors per die. The added functionality of memory in the back plane can have a substantial impact on cost particularly in PWM systems as transistor density can double again. Equation [1] predicts silicon yield below 30% for WXGA PWM backplanes with memory, as they need to use finer feature sizes to pack the extra transistor density required for this architecture.

The transistor density is doubled once more as the pixel array becomes more densely packed for 1920x1080 resolution backplane, and the silicon price can increase even further especially if smaller feature sizes are used. Published data on various LCOS architectures were accumulated including:

- Pixel array area
- Die area
- Silicon process feature size
- Circuitry per pixel (transistors, wires, capacitors) and their feature sizes

0.35 micron process										
12 transistors/pixel Analog										
	1280x720					1920x1080				
pixel array diagonal (in inches)	0.9	0.8	0.7	0.6	0.5	0.9	0.8	0.7	0.6	0.5
Silicon yield Estimate	95%	93%	91%	88%	83%	76%	70%	63%	53%	41%
die per wafer (w/ 2mm border)	76	92	114	144	187	76	92	114	144	187
yielded die per wafer (dpw)	72	86	104	127	156	58	64	72	77	76
LC Assembly yield (gross estimate)	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$
Wafer Cost (gross estimate)	wafer cost									
wafer level LCA cost	wafer level assembly cost									
die level cost (packaging, test cost per die)	$\beta * \text{number of die}$									
Relative Panel Cost	1.4	1.2	1.0	0.9	0.8	1.7	1.4	1.2	1.1	1.1

Figure 5: Estimate of relative cost of microdisplay panels made with 0.35 micron process and 12 transistors per pixel. Assumptions: a) LC assembly yield is lower for larger size die b) die level packaging cost and test is constant relative of size normalized to 0.7" diagonal panel.

Using this information some "typical" situations were modeled and the yield estimates extracted. First, using a 0.35 micron process and a somewhat typical transistor density of 12 transistors per pixel we arrive at the relative cost of various diagonal LCOS analog panels.

Next, using the same principal, we look at higher transistor densities and finer feature size processes. For these cases a) the silicon wafer processing cost increases, b) the silicon yield goes down and c) the packaging cost increases due to thermal dissipation requirements. These three factors have a dramatic impact on final estimated cost. As an example, we evaluate the case of 0.25 micron feature sizes and a higher transistor density to allow for PWM. The cost per panel more than doubles.

0.25 micron process					
24 transistors/pixel PWM					
	1280x720				
pixel array diagonal (in inches)	0.9	0.8	0.7	0.6	0.5
Silicon yield Estimate	63%	56%	47%	35%	22%
die per wafer (w/ 2mm border)	76	92	114	144	187
yielded die per wafer (dpw)	48	51	53	51	41
LC Assembly yield (gross estimate)	$\alpha - 10\%$	$\alpha - 5\%$	α	$\alpha + 5\%$	$\alpha + 10\%$
Wafer Cost (gross estimate)	wafer cost				
wafer level LCA cost	wafer level assembly cost				
die level cost (packaging, test cost per die)	$(\beta + \text{thermal}) * \text{number of die}$				
Relative Panel Cost	2.7	2.4	2.2	2.2	2.3

Figure 6: Using a conservative estimate on digital PWM processes having double the transistors of DRAM analog processes, the cost per panel is estimate to approximately double. Included is an increase in die packaging cost associated with the thermal management of the increased power consumption of the panel.

We see an approximate doubling in panel cost. Note that some defects are allowed in a display panel – a small number of bad pixels, particularly on the edges of the pixel area can be OK. The model used to estimate yield assumes the same fault tolerance for all architectures. An opportunity for yield improvement lies in redundant and fault tolerant architectures.

Will these cost differentials erode over time through leverage of Moore's Law: (the number of transistors in an integrated circuit will double every 18 months)? Moore's Law for LCOS is accompanied by factors in conflict with it a) die shrink vs. etendue b) increase power consumption/thermal packaging costs with smaller features, c) perceived greyscale using voltage transfer function of LC, or time-domain only modulation and d) decreased available voltage. All four of these factors have negative

implications on price/performance. The impact of Moore's Law to LCOS is, at best, less certain, and at worst shows more than an order of magnitude increase in product cost with silicon shrink.

3. Lumen Throughput

Philips, a leader in the production of ultra-high-pressure (UHP) mercury arc-lamps for projection displays has recently announced a 1.0mm arc gap is the minimum that can be achieved in the foreseeable future. The etendue coupling of a 1.0 mm gap is computed for various panel sizes at a constant F/# and depicted in the table below. Other light sources, like LEDs have less attractive etendue figures: the light lost as a function of silicon shrink is more pronounced. Only when lasers become the light source of choice for projection systems will silicon shrink and the march of Moore's law be unconstrained by etendue.

1.0 mm arc lamp coupling to LCOS panel							
F-number	0.4"	0.5"	0.6"	0.7"	0.8"	0.9"	cone angle (degrees)
2.4	26%	37%	44%	51%	56%	58%	11.3

The major factor affecting system cost and lumen throughput is the selection of a multi-panel (usually 3) or single-panel optical engine. The optical engine can be divided into 3 main components: 1) the light source, 2) the microdisplay panels and 3) everything else: all the optics to get the light on the panel, the polarization system, the color management system, the projection lens and the housing.

While all engines will vary *substantially* from the gross cost approximation presented here; it is used as a crude method to compare relative cost and impact of the final system. The lamp is about 20% of the engine cost. In a single panel system the panels are about 40% of the cost, and the rest of the engine comprises the remaining 40% of the cost. In the triple panel system (labeled 3p below), the panel cost and the light engine cost typically run higher. The net impact is that the triple panel optical engine is more expensive than the single panel engine by roughly ~150%.

	1p	3p
Lamp + Ballast	\$~0.6*Y	\$~0.6*Y
illuminator optics	\$~Y	\$~1.5*Y
PBS		
color-management system		
projection lens		
assembly cost		
mechanical		
LCOS chipset price	\$~Y	>~2*Y
TOTAL ENGINE COST	\$~2.6*Y	\$~4.1*Y

However, triple panel systems often produce more lumens: typically 300-400 lumens unlike single panel LCOS systems

which are currently limited to 200-300 lumens. Thus triple panel engines produce can produce 25-50% more lumens for ~50% higher cost.

Further, an analog 0.8" panel can be made for approximately 1.2X (as shown in Figure 5). Thus equating with the engine pricing table:

$$1.2X = Y/(1-GM\%)$$

where GM% is the gross margin or profit to the LCOS manufacturer. If we apply this logic to the triple panel chipset, for a triple panel engine, that costs ~50% more, but produces about 50% more lumens:

$$2.8X = \sim 2*Y/(1-GM\%)$$

We know that that three .7" panels (the commonly used panels in triple panel projection systems) cost about 1.0X per panel if analog (as shown in figure 5). Thus, the triple panel 0.7" analog system is competitive with the 0.8" single panel system in terms of lumens per dollar assuming similar gross margins.

For digital PWM three-panel systems, we estimate 2.2X per panel x 3 = 6.6X for the chipset (as shown in figure 6). 6.6X panel cost must than be compared to 4.7Y. Feeding this through our optical engine cost estimates above we conclude that a triple panel PWM digital engine costs about 250% more than then a single panel projection engine.

4. Grayscale

We have assessed cost so far without considering greyscale bit depth. Fundamentally, more information content can be conveyed in two dimensions (voltage and time) than in one dimension (time). Analog greyscale uses two dimensions (voltage and time), while PWM uses only one base dimension (time). In addition, the human visual system sees on a logarithmic scale: light 10X as intense appears 2X as bright. Thus the liquid crystal material properties – the voltage transfer function – can be made to match the properties of the human visual system and thus reduce the bit depth required for excellent greyscale rendition: lowering both cost and transistor density. With a binary pulse width modulation scheme and a linear clock, increased bit depth is required to achieve the same perceptual grey scale. The increased bit depth requires even higher transistor density impacting the LCOS panel cost even further.

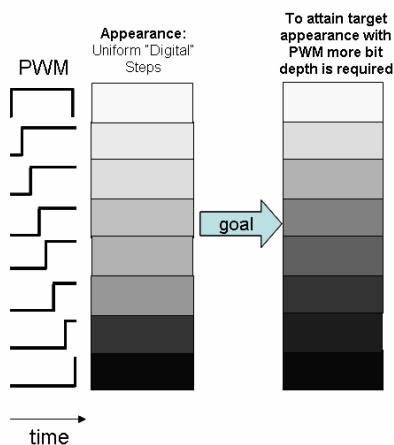


Figure 7: On the left hand side pulse width modulation is depicted. A temporal field is divided into eight uniform time segments. When no voltage is applied (as in the lower left of the column labeled “appearance”) the image appears black, when the voltage is ‘on’ for the entire field it appears white as at the top of the column labeled “appearance”. If the voltage is ‘on’ for part of the field and ‘off’ for the part of the field the human visual system can’t see the fast transition and interprets this as grey. Because the eye perceives brightness on a logarithmic intensity scale, smaller steps are required in the blacks and dark greys when using PWM. Alternatively, using an DRAM architecture and voltage modulation of the liquid crystals, the liquid crystal voltage transfer function can be made to match the logarithmic response of the human visual system allowing the use of lower bit depth to represent better grey shades than in PWM where the dark greys typically exhibit an artifact called contouring.

5. Conclusions

Costs and yields are generally not discussed in scientific papers for a) proprietary reasons b) they change over time and c) costs at are generally not considered “interesting” to the scientific community. While these costs will change over time, the silicon processes used for LCOS have changed little over the last five years. Silicon design has a profound impact on the optical engine cost and performance. In this paper we touched on three major areas where this impact is strongest: LCOS yield, optical engine cost and perceived greyscale bit-depth. Best theoretical transistor densities for PWM silicon backplanes were compared to typical transistor densities for “analog” silicon LCOS backplanes. The analog systems showed large cost and performance advantages: less than half the cost with better grayscale performance than PWM “digital” LCOS. LCOS analog backplanes are typically used in single panel optical engines, while LCOS digital backplanes are typically used in the triple systems, and thus the cost impact is compounded in that single panel systems are also less expensive than triple panel optical engines.

6. Acknowledgements

The author would like to thank Misha Bolotski for several helpful discussions.

7. References

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